

Attorney Docket: 33851/41886  
PATENT



APR 27 2006

AF/1FW

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Inventor	Dustin A. Woodbury	Confirmation No.	6517
Serial No.	10/798,559	Art Unit:	2818
Filing Date	March 12, 2004	Examiner	LE, Thao P.

Title: **METHOD AND STRUCTURE FOR NON-SINGLE-POLYCRYSTALLINE  
CAPACITOR IN AN INTEGRATED CIRCUIT**

**AMENDMENT AFTER FINAL**

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In response to the official Final Patent Office action dated January 31, 2006, please amend the claims as shown in the attached Claims Summary.

Claims 1-12 stand rejected under 35 U.S.C. 103(a) as being unpatentable over by Chi, U.S. Patent 5,173,437 in view of Applicants Admitted Prior Art. This rejection is respectfully traversed.

Claim 1 is directed to a method of forming a capacitor in an integrated circuit including forming a first non-single-crystalline layer on a gate dielectric layer on a surface of the integrated. A capacitor dielectric layer is formed on the first non-single-crystalline layer and a second non-single-crystalline layer is formed on the capacitor dielectric layer. Portions of the second non-single-crystalline layer is removed to define a top plate of the capacitor. A mask is formed over the top plate and exposed portions of the capacitor dielectric layer with an opening. The mask is used to etch and simultaneously remove portions of the capacitor dielectric layer and portions of the first non-single-crystalline layer to define a bottom plate of the capacitor after a top plate is defined on the gate dielectric.

Claim 1 as amended is the combination of claim 1 and cancelled claims 7 and 8 and thus are not considered to raise new issues after final.

The process Chi, as noted in the office, uses the top gate as the mask for removing and defining the capacitor dielectric 58. This is performed before the mask 72 which is used to define the bottom plate 80. As noted, Claim 1 specifically requires that the mask is used to